

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,888,243 B2
APPLICATION NO. : 09/964462
DATED : May 3, 2005
INVENTOR(S) : Yasuo Yamaguchi

Page 1 of 18

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The title page should be deleted to appear as per attached title page.

Signed and Sealed this

Eighth Day of January, 2008

A handwritten signature in black ink, reading "Jon W. Dudas". The signature is stylized, with a large, looped initial "J" and a cursive "Dudas".

JON W. DUDAS
Director of the United States Patent and Trademark Office

(12) **United States Patent**
Yamaguchi

(10) Patent No.: **US 6,888,243 B2**
(45) Date of Patent: **May 3, 2005**

(54) **SEMICONDUCTOR DEVICE**

(75) Inventor: Yasuo Yamaguchi, Tokyo (JP)

(73) Assignee: Renesas Technology Corp., Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 351 days.

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Primary Examiner—David L. Tibbott

Assistant Examiner—Lourdes Cruz

(74) Attorney, Agent, or Firm—Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

(21) Appl. No.: 09/964,462

(22) Filed: Sep. 28, 2001

(65) Prior Publication Data

US 2002/0105079 A1 Aug. 8, 2002

(30) Foreign Application Priority Data

Feb. 6, 2001 (JP) 2001-029807

(51) Int. Cl.⁷ H01L 23/48

(52) U.S. Cl. 257/748; 257/758; 257/774;
257/471

(58) Field of Search 257/748, 758,
257/280, 613, 471, 774

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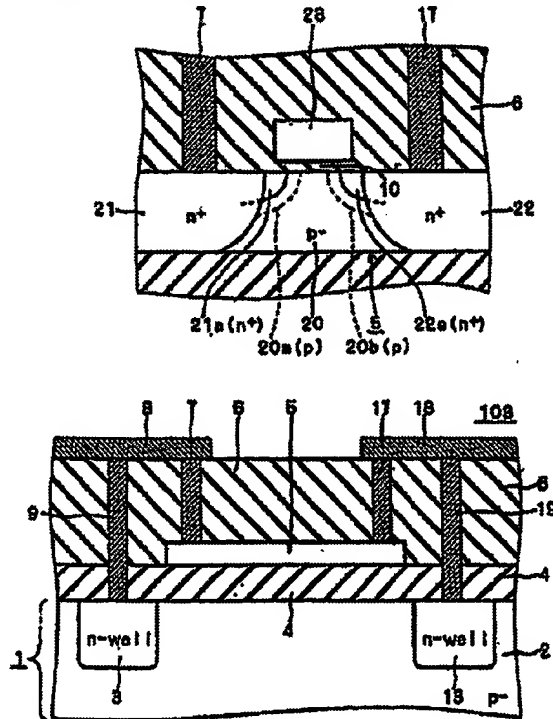
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(57) **ABSTRACT**

To improve the radiation property without inhibiting miniaturization of the device, heat generated at a heat generating layer (5) is radiated to a substrate (1) via plugs (7, 17), wiring layers (8, 18), and plugs (9, 19). A cross sectional along the principal plane of the substrate (1) of the plugs (7, 9, 17, 19) is set to be a rectangle, and the long sides of the rectangle are parallel to the direction perpendicular to the direction connecting one end and the other end of the heat generating layer (5). Between the plugs (9, 19) and the semiconductor layer (2) is interposed n-type semiconductor layers (3, 13).

20 Claims, 12 Drawing Sheets



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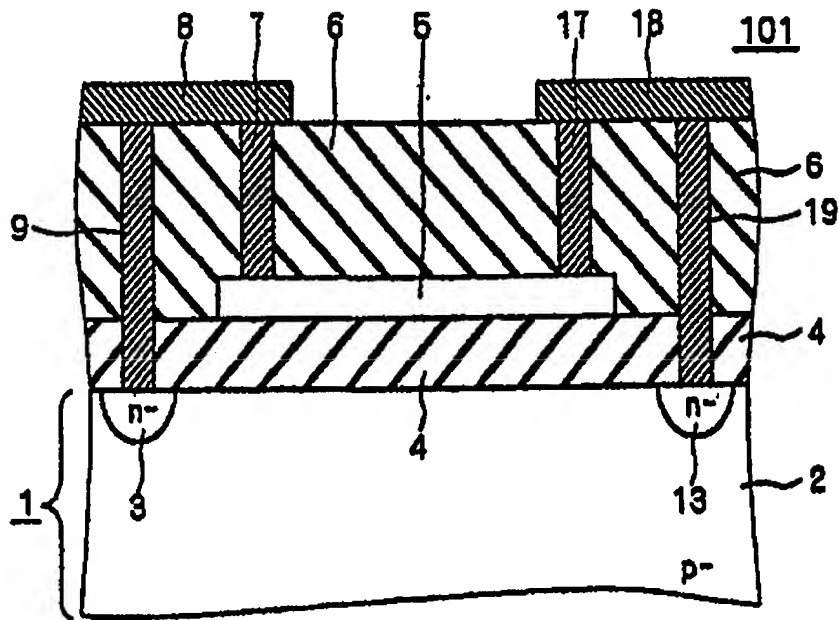
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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the drawings, please replace figure 1 with the following figure 1:

FIG. 1



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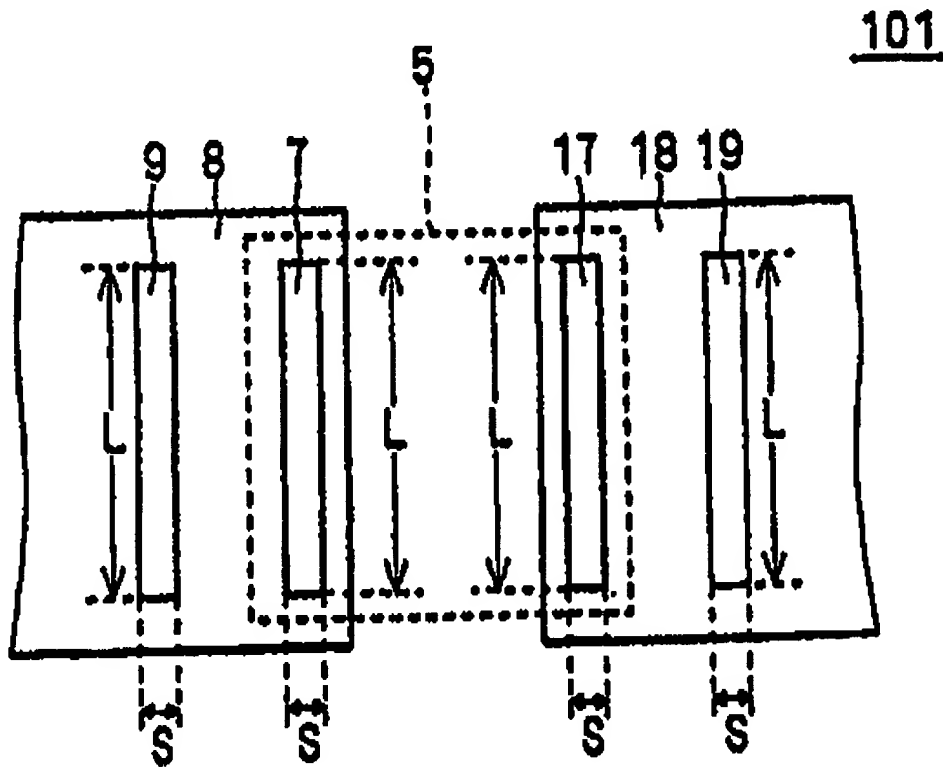
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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the drawings, please replace figure 2 with the following figure 2:

FIG. 2



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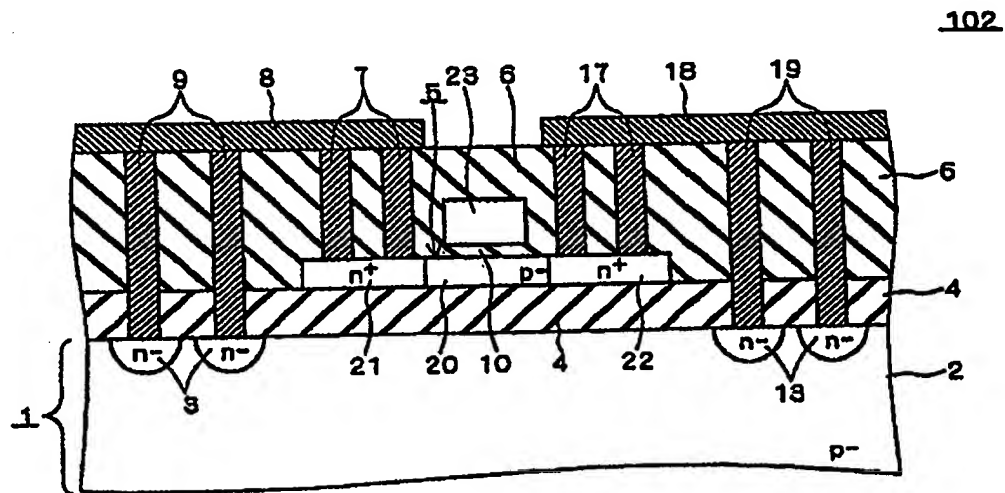
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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the drawings, please replace figure 3 with the following figure 3:

FIG. 3



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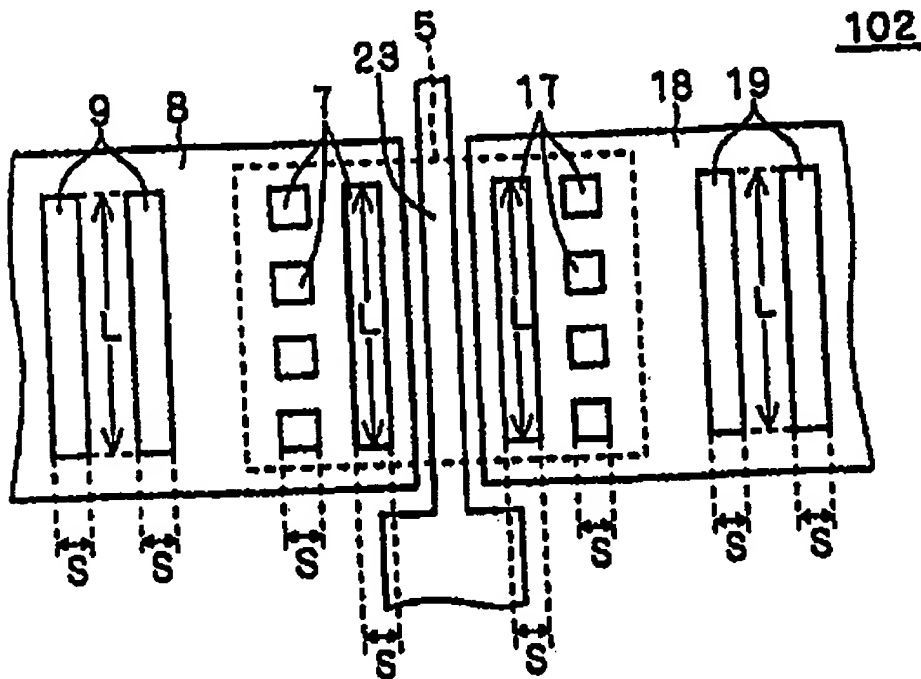
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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the drawings, please replace figure 4 with the following figure 4:

FIG. 4



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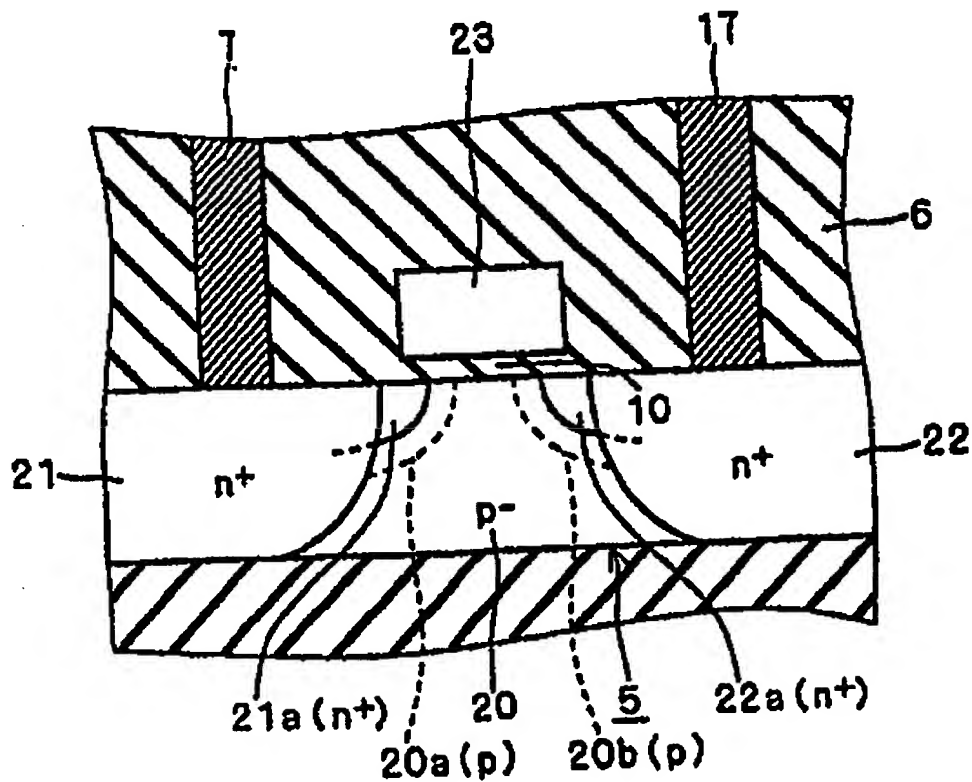
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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the drawings, please replace figure 5 with the following figure 5:

FIG. 5



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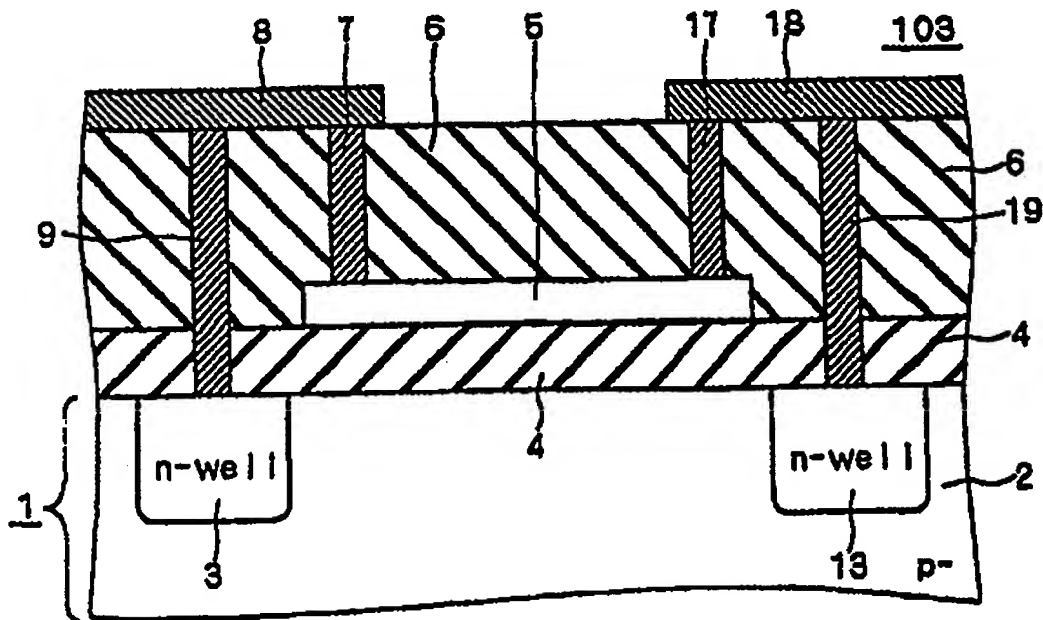
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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the drawings, please replace figure 6 with the following figure 6:

F / G. 6



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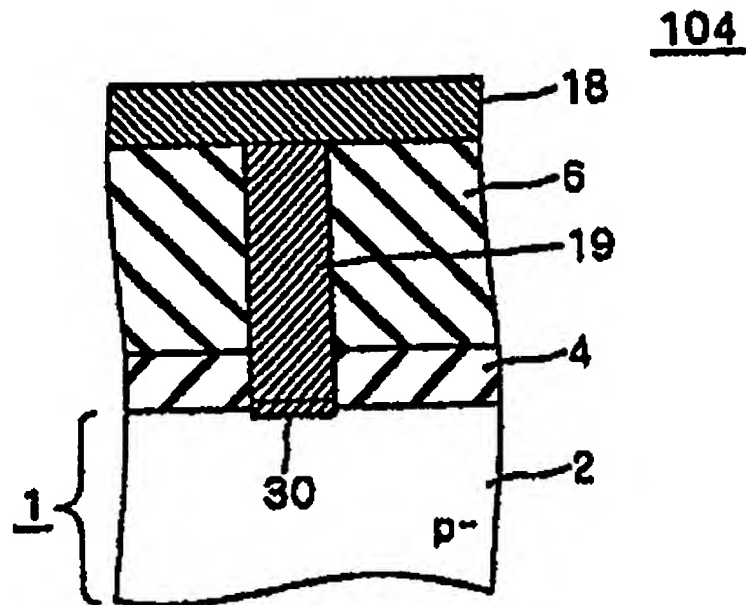
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INVENTOR(S) : Yasuo Yamaguchi

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the drawings, please replace figure 7 with the following figure 7:

FIG. 7



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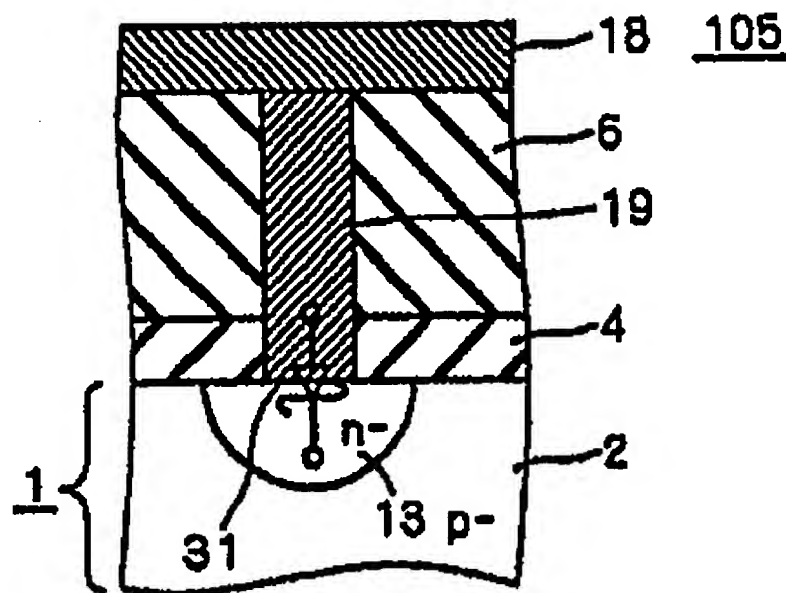
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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the drawings, please replace figure 8 with the following figure 8:

FIG. 8



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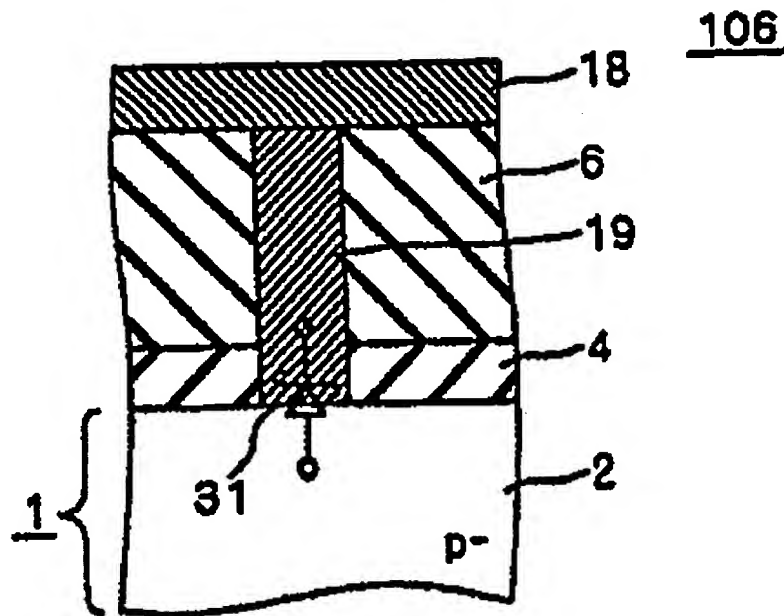
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DATED : May 3, 2005
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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the drawings, please replace figure 9 with the following figure 9:

FIG. 9



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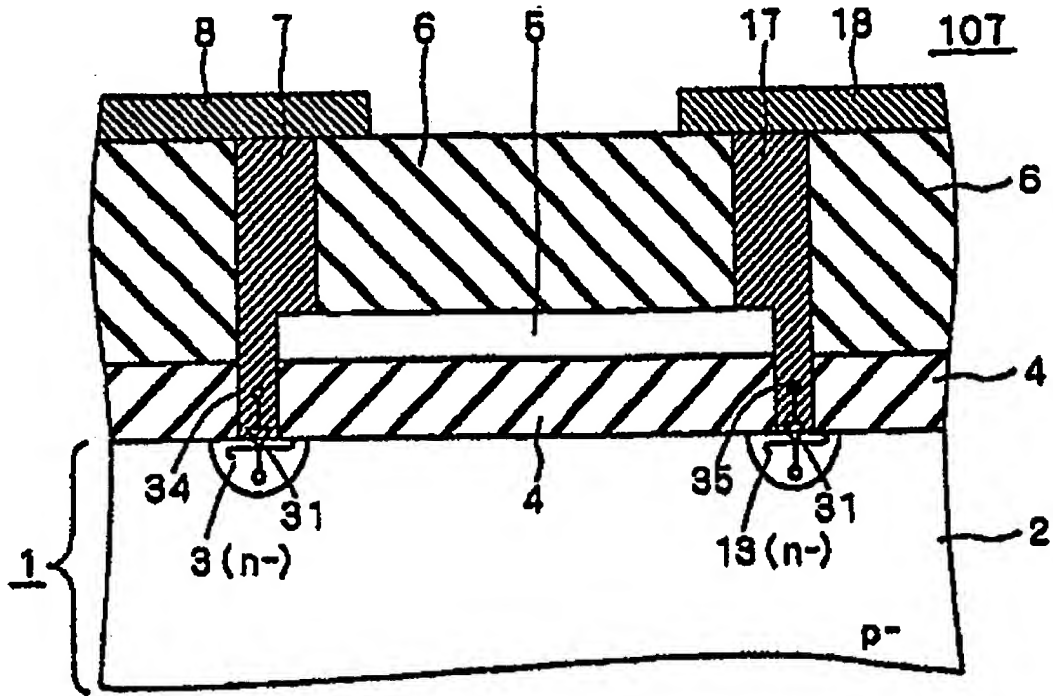
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INVENTOR(S) : Yasuo Yamaguchi

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In the drawings, please replace figure 10 with the following figure 10:

FIG. 10



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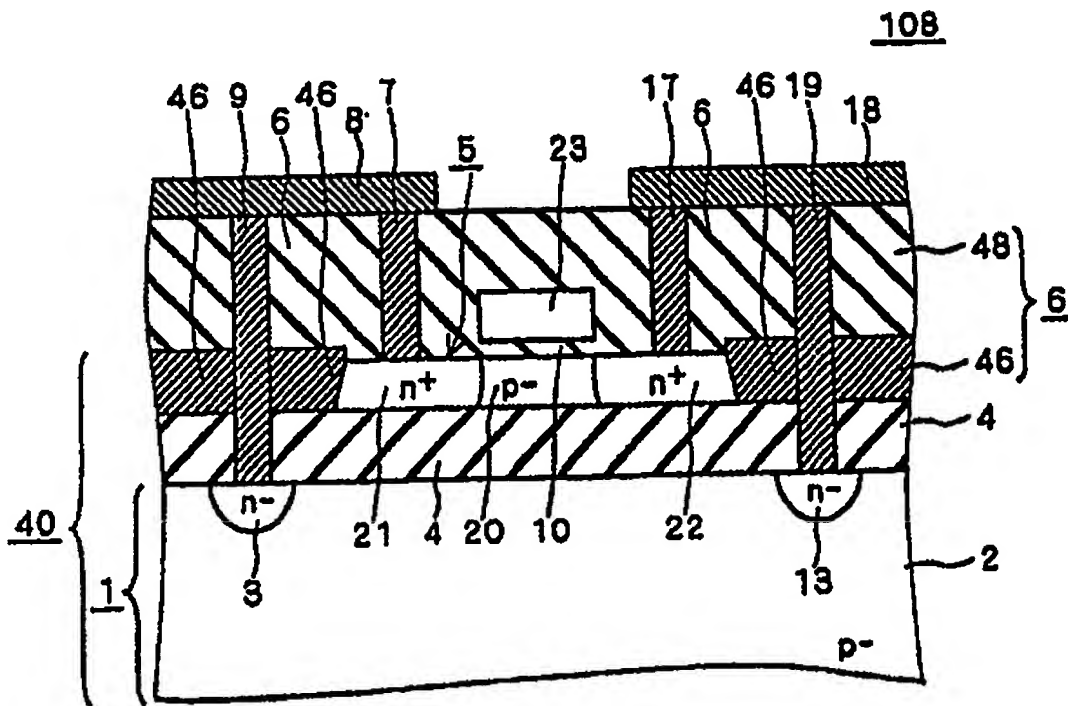
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In the drawings, please replace figure 11 with the following figure 11:

FIG. 11



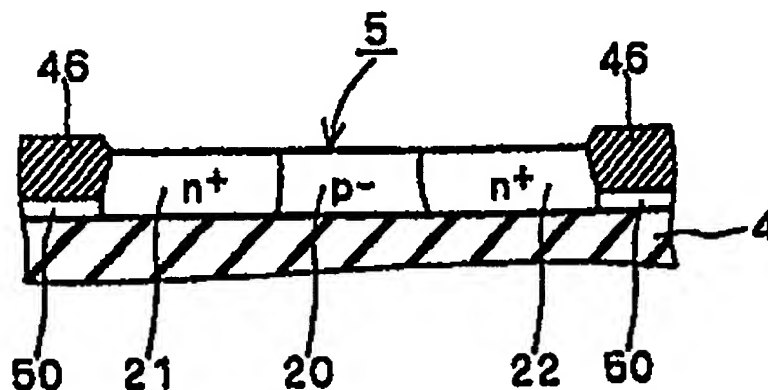
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In the drawings, please replace figure 12 with the following figure 12:

F/G. 12



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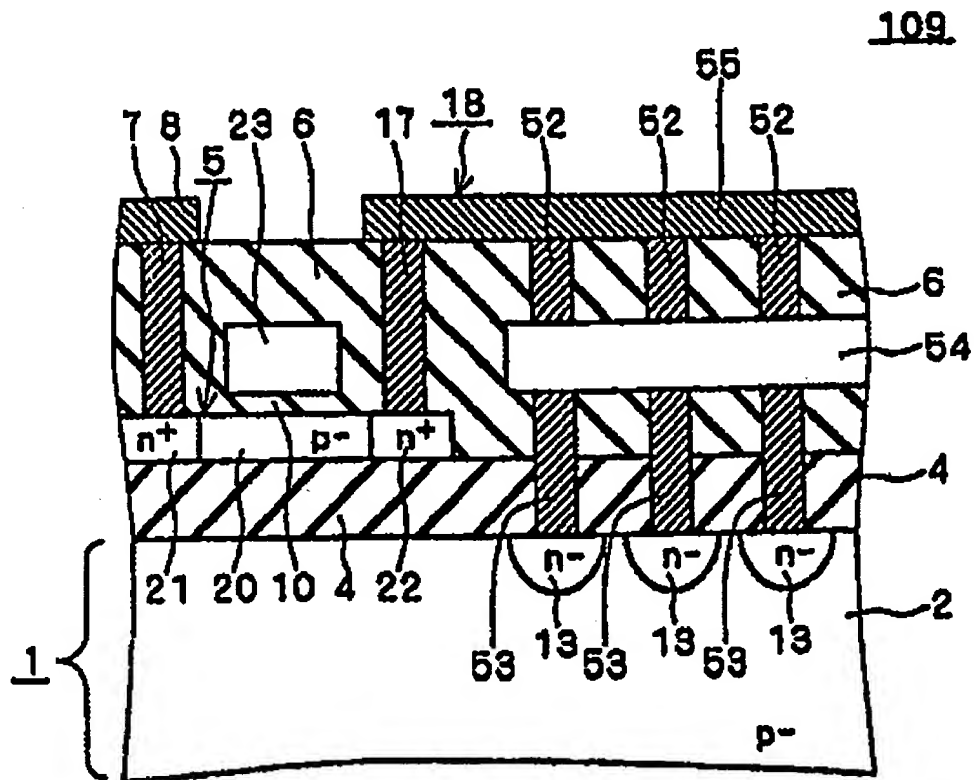
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FIG. 13



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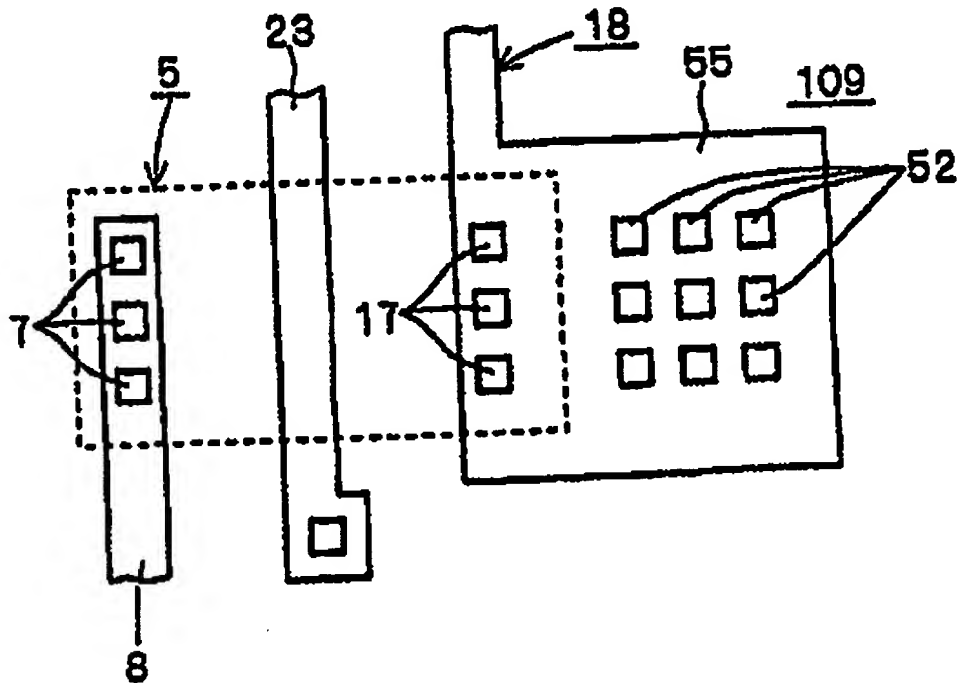
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DATED : May 3, 2005
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In the drawings, please replace figure 14 with the following figure 14:

FIG. 14



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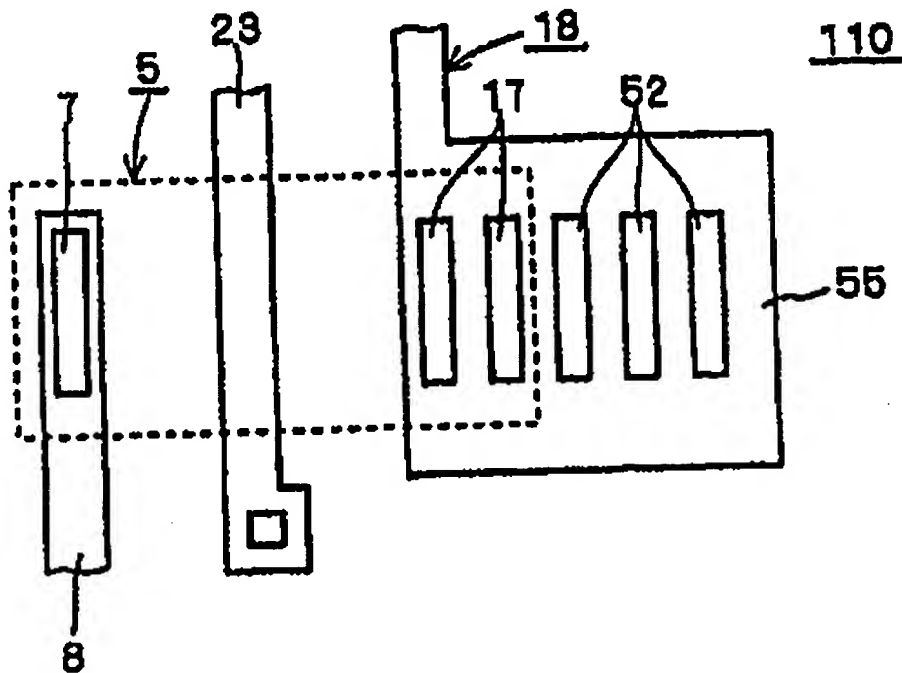
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In the drawings, please replace figure 15 with the following figure 15:

FIG. 15



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In the drawings, please replace figure 16 with the following figure 16:

FIG. 16

